REMARKS

Claims 1 through 16, 19, through 24, 26 through 41, and 44 through 49 are currently pending in the application.

Claims 17, 18, 25, 42, 43, and 50 have been withdrawn as being drawn to a non-elected species.

Claims 1 through 16, 19, through 24, 26 through 41, and 44 through 49 stand rejected.

Applicant has amended independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 and requests reconsideration of the application as amended herein.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent 5,864,178 to Yamada et al.

Claims 1 through 3, 5 through 8, 10 through 12, 14 through 16, 20, 21, 23, 24, 26 through 28, 30 through 33, 35 through 37, 39 through 41, and 45 through 49 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamada et al. (U.S. Patent 5,864,178). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Turning to the cited prior art Yamada et al. reference, described is a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing filler. In FIGS. 56A through 56D a semiconductor chip 201 is mounted on a wiring circuit board 202 using bumps 203 with the semiconductor chip 201 having a layer of a first resin 204 constituting a laminate of encapsulation resin, a second layer of resin 205 on the wiring circuit board 202 constituting a laminate of encapsulation resin, a third encapsulation resin 206 constituting a laminate of encapsulation resin applied to a portion of the second layer of resin 205, a polymer

film 207 formed on the semiconductor chip 201, and a polymer film 208 formed on the wiring circuit board 202. Nowhere does Yamada et al. describe the semiconductor chip 201 having at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wetable by a polymeric material. At best, Yamade et al. describe that solely the first layer of encapsulation resin 204, second layer of encapsulation resin 205, and third encapsulation resin 206 may include a silane coupling agent therein mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board as a wetting agent layer. Nowhere in the Yamada et al. reference is there any description whatsoever directed to any of the encapsulation resins 204, 205, and 206 acting as a wetting agent under any circumstances.

Additionally, nowhere in the specification of the present application does Applicant describe the wetting agents of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane as resins. They are not resins of any type. Additionally, Applicant asserts that nowhere has any prior art been cited in the application to show that silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane are resins whatsoever. At best, the cited prior art describes such compounds as mixed with resins, not separately applied. Applicant asserts that any such characterization of any of the cited prior art that silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane are resins is incorrect and absolutely unfounded.

Applicant asserts that the Yamada et al. reference does not and cannot anticipate the presently claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 under 35 U.S.C. § 102 because the Yamada et al. reference does not identically describe, either expressly or inherently, each and every element of the presently claimed inventions in as complete detail as is contained in the claims. For instance, Applicant asserts that the Yamada et al. reference does not identically describe the elements of the presently claimed inventions set forth in independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for "the semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thickness thereon comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active

surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent located on a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material, the underfill material essentially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of about a monolayer and wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", and "a wetting agent layer provided on

said active surface of said semiconductor die and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material".

In contrast to the claimed inventions, Applicant asserts that nowhere, either expressly or inherently, does the Yamada et al. reference describe a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Yamada et al. reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin. Therefore, the Yamada et al. reference cannot and does not anticipate under 35 U.S.C. § 102 the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,864,178 to Yamada et al. in View of U.S. Patent No. 6,180,696 to Wong et al.

Claims 4, 9, 13, 19, 22, 29, 34 28, and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al. (U.S. Patent No. 5,864,178) in view of Wong et al. (U.S. Patent No. 6,180,696). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable

> expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Turning to the cited prior art Yamada et al. reference, described is a semiconductor device comprising a wiring circuit board and a semiconductor chip mounted through a bump electrode on the circuit board, a space between the circuit board and the semiconductor chip as well as a periphery of the semiconductor chip being encapsulated with a resin containing filler. In FIGS. 56A through 56D a semiconductor chip 201 is mounted on a wiring circuit board 202 using bumps 203 with the semiconductor chip 201 having a layer of a first resin 204 constituting a laminate of encapsulation resin, a second layer of resin 205 on the wiring circuit board 202 constituting a laminate of encapsulation resin, a third encapsulation resin 206 constituting a laminate of encapsulation resin applied to a portion of the second layer of resin 205, a polymer film 207 formed on the semiconductor chip 201, and a polymer film 208 formed on the wiring circuit board 202. Nowhere does Yamada et al. describe the semiconductor chip 201 having at least a portion of said active surface having a wetting agent layer of about a monolayer thick thereon, said wetting agent layer wetable by a polymeric material. At best, Yamade et al. describe that solely the first layer of encapsulation resin 204, second layer of encapsulation resin 205, and third encapsulation resin 206 may include a silane coupling agent therein mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. Nowhere in the Yamada et al. reference is there any description whatsoever directed to any of the encapsulation resins 204, 205, and 206 acting as a wetting agent under any circumstances.

The Wong reference teaches or suggests an epoxy base polymeric composition/formulation with a curing peak temperature ranging from 180°C to 240°C, suitable rheologic characteristics and excellent fluxing activity, which meets the requirements of the no-flow underfilling process for low melting point solder bumps such as with eutetic tin/lead alloy. The epoxy base polymeric composition/formulation includes a silane coupling agent to improve the adhesion between a semiconductor die and the under fill material. The Wong reference does

not teach or suggest the use of a silane coupling agent except as part of the epoxy base polymeric composition/formulation.

Applicant asserts that no combination of the Yamada et al. reference and the Wong reference establishes a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 because, at the very least, any combination of the cited prior art fails to teach or suggest all of the claim limitations of the inventions set forth in such independent claims.

For instance, Applicant asserts that any combination of the Yamada et al. reference and the Wong reference fails to teach the claim limitations of the inventions set forth in independent claims 1, 6, 10, 14, 20, 23, 26, 31, 35, 39, 45, and 48 calling for for "the semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer thickness thereon comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device, said wetting agent layer having a thickness of about a monolayer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent located on a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on at least a portion of said active surface of said semiconductor device comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material, the underfill material essentially filling a volume between said wetting agent layer and said upper surface of said substrate", "a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no

substantial degradation thereof during one of a solder reflow process and a curing process for a material", "the semiconductor die having an active surface, at least a portion of said active surface having a wetting agent layer of about a monolayer in thickness thereon, said wetting agent layer wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on said active surface of said semiconductor die, said wetting agent layer having a thickness of about a monolayer and wetable by a polymeric material, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", "a wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material", and "a wetting agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate, said wetting agent layer comprising a layer of solely a silane-based material which undergoes no substantial degradation thereof during one of a solder reflow process and a curing process for a material".

In contrast to the claimed inventions, Applicant asserts that nowhere does any combination of the Yamada et al. reference and the Wong reference teach or suggest a wetting agent used on a portion of a semiconductor device, semiconductor die, or substrate in any manner. At best, the Wong reference discusses the use of silane coupling agent mixed with the other components forming the layer of encapsulation resin. The silane coupling agent is only used in the formulation of the encapsulation resin itself, not separately applied to either the semiconductor chip or the wiring circuit board. The claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are not directed to the use of a silane coupling agent in the formulation of an encapsulation resin. Therefore, the Yamada et al. reference and the Wong reference cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39,

45, and 48. Accordingly, independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48 are allowable as well as the dependent claims therefrom.

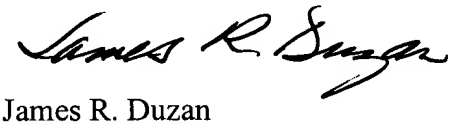
Yet further, the Yamada et al. reference fails to teach or suggest a wetting agent layer of about a monolayer thick that is wetable by a polymeric material to teach or suggest the presently claimed inventions under 35 U.S.C. § 103.

In contrast to the claimed inventions of independent claims 1, 6, 10, 14, 20, 23, 25, 31, 25, 39, 45, and 48, the Yamada et al. does not disclose a monolayer thick wetting agent layer having the specific wetting properties as recited in presently amended claims 1 and 26. Neither does the Wong reference teach or suggest a wetting agent layer of about a monolayer thick. Additionally, no combination of the Yamada et al. reference and the Wong reference teaches or suggests a wetting agent layer of about a monolayer thick. Therefore, independent claims 1, 26, and 31 and claims depending therefrom are not taught or suggested by any combination of the Yamada et al. reference and the Wong reference.

CONCLUSION

Claims 1 through 16, 19, through 24, 26 through 41, and 44 through 49 are believed to be allowable for the reasons set forth herein, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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